TDK SEMICONDUCTOR CORP.

73K222AL
V.22, V.21, Bell 212A, 103
Single-Chip Modem

June 2001

DESCRIPTION

The 73K222AL is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22, V.21 and Bell 212A compatible modem, capable of 1200 bit/s full-duplex operation over dial-up lines. The 73K222AL is an enhancement of the 73K212L/AL single-chip modem which adds V.22 and V.21 modes to the Bell 212A and 103 operation of the 73K212AL. In Bell 212A mode, the 73K222AL provides the normal Bell 212A and 103 functions and employs a 2225 Hz answer tone. The 73K222AL in V.22 mode produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows 600 bit/s V.22 or 0-300 bit/s V.21 operation. The 73K222AL integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28-pin DIP, and 28-pin PLCC configuration. The 73K222AL operates from a single +5V supply. The 73K222AL is a new version replacing the 73K222L. The 73K222AL should be specified for all new designs.

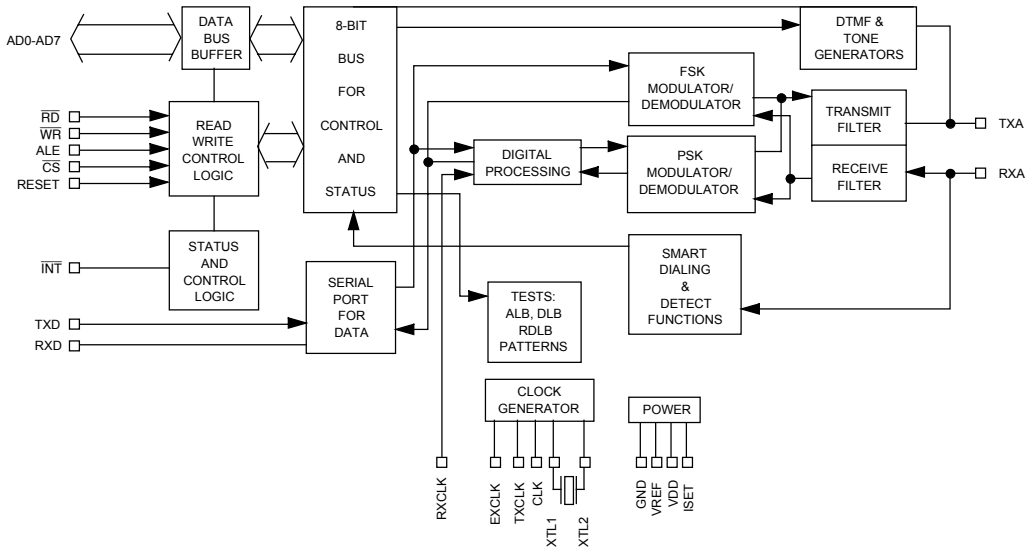
The 73K222AL includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor and a tone generator capable of tone required for European applications.

(continued)

FEATURES

- **One-chip CCITT V.22, V.21, Bell 212A and Bell 103 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)**
- **Pin and software compatible with other TDK Semiconductor Corporation K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation including V.22 extended overspeed**
- **Call progress, carrier, precise answer tone (2100 or 2225 Hz), and long loop detectors**
- **DTMF, and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 60 mW @ 5V**
- **Single +5 volt supply**
- **PLCC and PDIP packages**

BLOCK DIAGRAM



This datasheet has been downloaded from http://www.digchip.com at this page

DESCRIPTION (continued)

This device supports V.22 (except mode v) and V. 21 modes of operation, allowing both synchronous and asynchronous communications. Test features such as analog loop, digital loop, and remote digital loopback are supported. Internal pattern generators are also included for self-testing. The 73K222AL is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The 73K222AL is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The 73K222AL is part of TDK Semiconductor Corporation's K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The 73K222AL includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data within a ±0.01% rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± 0.01% (± 0.01% is required synchronous data rate accuracy).

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 times N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The 73K222AL modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a

2400 Hz carrier (originate mode or ALB answer mode). The 73K222AL uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space), or 1650 and 1850Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 or V.21 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the 73K222AL control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the addressed register occurs on the rising edge of $\overline{WR}$. This interface mode is also supported in the 28-pin packages. See serial control interface pin description.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ± 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	TYPE	DESCRIPTION
GND	28	I	System Ground.
VDD	15	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to GND.
VREF	26	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to ground.
ISET	24	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	I	Read. A low requests a read of the 73K222AL internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (continued)

NAME	28-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	I	Write. A low on this informs the 73K222AL that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	I	Read. A low on this input informs the 73K222AL that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	I	Write. A low on this input informs the 73K222AL that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
NOTE: The serial control mode is provided by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become the address only. See timing diagrams on page 20.			

PIN DESCRIPTION (continued)

DTE USER

NAME	28-PIN	TYPE	DESCRIPTION
EXCLK	19	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to on the TXD pin. Also used for serial control interface.
RXCLK	23	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	O/ Weak Pull-up	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	I	Received modulated analog signal input from the telephone line interface.
TXA	16	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. In parallel mode the address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the 73K222AL internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANS TONE
CONTROL REGISTER 2 CR2	100	X	X	X	THESE REGISTER LOCATIONS ARE RESERVED FOR				X
CONTROL REGISTER 3 CR3	101	X	X	X	USE WITH OTHER K-SERIES FAMILY MEMBERS				X
ID REGISTER ID	110	ID	ID	ID	ID	X	X	X	X

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined, mask in software

REGISTER ADDRESS TABLE

REGISTER		ADDRESS AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
			DATA BIT NUMBER							
CONTROL REGISTER 0	CR0	000	MODULATION OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
CONTROL REGISTER 1	CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	X	X	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER	TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER/ TONE
ID REGISTER	10	110	ID	ID	ID	ID	X	X	X	X

CONTROL REGISTER 0:
- MODULATION OPTION: 0 = 1200 BIT/S DPSK; 1 = 600 BIT/S DPSK; 0 = BELL 103 FSK; 1 = V.21 FSK
- TRANSMIT MODE 3 – TRANSMIT MODE 0: 0000 = PWR DOWN; 0001 = INT SYNCH; 0010 = EXT SYNCH; 0011 = SLAVE SYNCH; 0100 = ASYNCH 8 BITS/CHAR; 0101 = ASYNCH 9 BITS/CHAR; 0110 = ASYNCH 10 BITS/CHAR; 0111 = ASYNCH 11 BITS/CHAR; 1100 = FSK
- TRANSMIT ENABLE: 0 = DISABLE TXA OUTPUT; 1 = ENABLE TXA OUTPUT
- ORIGINATE/ ANSWER: 0 = ANSWER; 1 = ORIGINATE

CONTROL REGISTER 1:
- TRANSMIT PATTERN 1 – TRANSMIT PATTERN 0: 00 = TX DATA; 01 = TX ALTERNATE; 10 = TX MARK; 11 = TX SPACE
- ENABLE DETECT INTERRUPT: 0 = DISABLE; 1 = ENABLE
- BYPASS SCRAMBLER: 0 = NORMAL; 1 = BYPASS SCRAMBLER
- CLK CONTROL: 0 = XTAL; 1 = 16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY
- RESET: 0 = NORMAL; 1 = RESET
- TEST MODE 1 – TEST MODE 0: 00 = NORMAL; 01 = ANALOG LOOPBACK; 10 = REMOTE DIGITAL LOOPBACK; 11 = LOCAL DIGITAL LOOPBACK

DETECT REGISTER:
- RECEIVE DATA: OUTPUTS RECEIVED DATA STREAM
- UNSCR. MARKS – LONG LOOP: 0 = CONDITION NOT DETECTED; 1 = CONDITION DETECTED

TONE CONTROL REGISTER:
- RXD OUTPUT CONTROL: RXD PIN; 0 = NORMAL; 1 = TRI STATE
- TRANSMIT GUARD/ TONE: 0 = OFF; 1 = ON
- TRANSMIT ANSWER TONE: 0 = OFF; 1 = ON
- TRANSMIT DTMF: 0 = DATA; 1 = TX DTMF
- DTMF3 – DTMF0/ GUARD/ ANSWER/ TONE: 4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS
- DTMF0/ GUARD/ ANSWER/ TONE: 0 = 2225 Hz A.T. 1800 Hz G.T.; 1 = 2100 Hz A.T. 500 Hz G.T.

00XX = 73K212AL, 322L, 321L
01XX = 73K221AL, 302L
10XX= 73K222AL, 222BL
1100 = 73K224L
1110 = 73K324L
1111 = 73K224BL
1101 = 73K324BL

X = Undefined, mask in software

CONTROL REGISTER 0

CR0 000	D7	D6	D5	D4	D3	D2	D1	D0
	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to allow Answer Tone and DTMF Transmission.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	Selects power down mode. All functions disabled except digital interface.
		0 0 0 0	
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a “0.”

CONTROL REGISTER 0 (continued)

CR0 000	D7	D6	D5	D4	D3	D2	D1	D0
	MODUL. OPTION	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION			DESCRIPTION
D7	Modulation Option	D7	D5	D4	Selects:
		0	0	X	DPSK mode at 1200 bit/s.
		1	0	X	DPSK mode at 600 bit/s.
		0	1	1	FSK Bell 103 mode.
		1	1	1	FSK CCITT V.21 mode.
					X = Don't care

CONTROL REGISTER 1

CR1 001	D7	D6	D5	D4	D3	D2	D1	D0
	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION		DESCRIPTION
D1, D0	Test Mode	D1	D0	
		0	0	Selects normal operating mode.
		0	1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1	0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1	1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0		Selects normal operation.
		1		Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0		Selects 11.0592 MHz crystal echo output at CLK pin.
		1		Selects 16 X the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	Selects normal data transmission as controlled by the state of the TXD pin.
		0 0	
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.

DETECT REGISTER (continued)

DR 010	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Detect	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in originate mode for detection of answer tone. For CCITT answer tone detection, bit D0 of the Tone Register must be set to a 1.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the receive channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Not Used	Undefined	Not used. Mask in software.

TONE REGISTER

TR 011	D7	D6	D5	D4	D3	D2	D1	D0
	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 0 0 0	Detects 2225 Hz in originate mode.
		X 1 0 0	Transmits 2225 Hz in answer mode (Bell).
		X 0 0 1	Detects 2100 Hz in originate mode.
		X 1 0 1	Transmits 2100 Hz in answer mode (CCITT).
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK +1.0% -2.5%.
		0 1	Asynchronous DPSK +2.3% -2.5%.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:
D4	Transmit DTMF	0	Disable DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	D5 D4 D0	D5 interacts with bits D4 and D0 as shown.
		0 0 X	Disables answer tone generator.
		1 0 0	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.
		1 0 1	Likewise a 2100 Hz answer tone will be transmitted.

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE REGISTER (continued)

TR 011	D7	D6	D5	D4	D3	D2	D1	D0
	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

ID 110	D7	D6	D5	D4	D3	D2	D1	D0
	ID	ID	ID	ID	X	X	X	X

BIT NO.	NAME	CONDITION				DESCRIPTION
D7, D6, D5, D4	Device Identification Signature	D7	D6	D5	D4	Indicates Device:
		0	0	X	X	73K212AL, 73K321L, 73K322L
		0	1	X	X	73K221AL or 73K302L
		1	0	X	X	73K222AL, 73K222BL
		1	1	0	0	73K224L
		1	1	1	0	73K324L
		1	1	1	1	73K224BL
		1	1	0	1	73K324BL
D3-D0	Not Used	Undefined				Mask in software

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD + 0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics; from pin to GND			40	pF
XTL2 Load Capacitor				20	

ELECTRICAL SPECIFICATIONS (continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Current	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATIONS (continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11.5	-10.0	-9	dBm0
FSK Mod/Demod					
Output Frequency Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Frequency Accuracy		-0.25		+0.25	%
Output Amplitude	Low Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, DPSK Mode	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Carrier Detect	DPSK or FSK				
Threshold	Receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	Not in V.21 mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Frequency Range		-2.5		+2.5	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 db in 0.3 to 3.4 kHz	10			kΩ
				50	pF
Spurious Frequency Comp.	Frequency = 76.8 kHz			-39	dBm0
	Frequency = 153.6 kHz			-45	dBm0
TXA pin Output Impedance			200	300	Ω
Clock Noise	TXA pin; 76.8 kHz			1.0	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

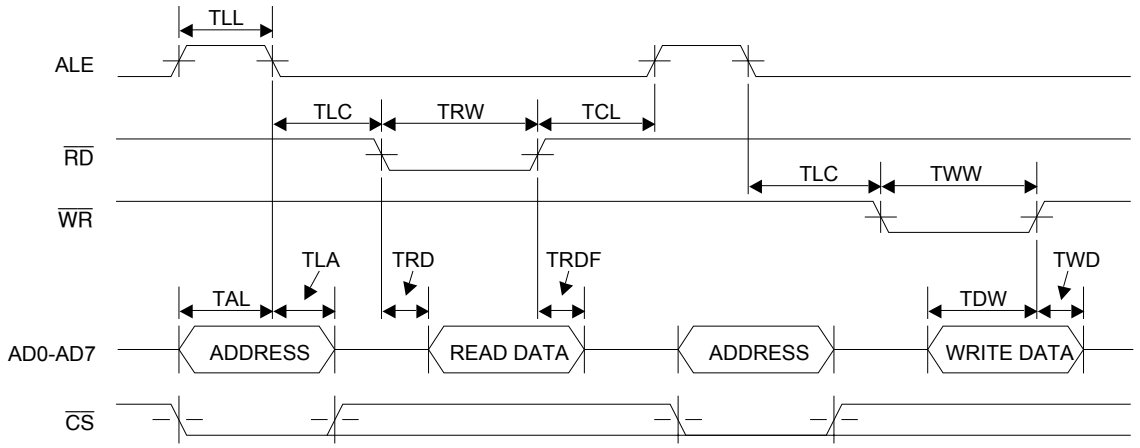
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Guard Tone Generator					
Tone Accuracy	550 Hz				
	1800 Hz	-20		+20	Hz
Tone Level (Below DPSK Output)	550 Hz	-4.0	-3.0	-2.0	dB
	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion 700 to 2900 Hz	550 Hz			-50	dB
	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Address setup before ALE Low	12			ns
TLA $\overline{CS}$	$\overline{CS}$ hold after ALE low	0			ns
TLA ADDR	Address hold after ALE low	10			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	10			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	0			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	15			ns
TRDF	Data float after $\overline{RD}$ High			50	ns
TRW	$\overline{RD}$ width	50			ns
TWW	$\overline{WR}$ width	50			ns
TDW	Data setup before $\overline{WR}$ High	15			ns
TWD	Data hold after $\overline{WR}$ High	12			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

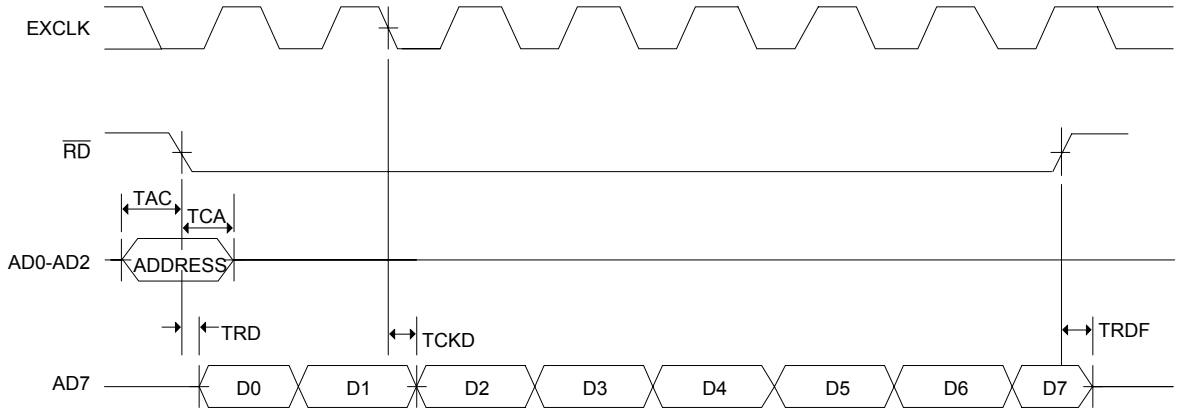
NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

TIMING DIAGRAMS

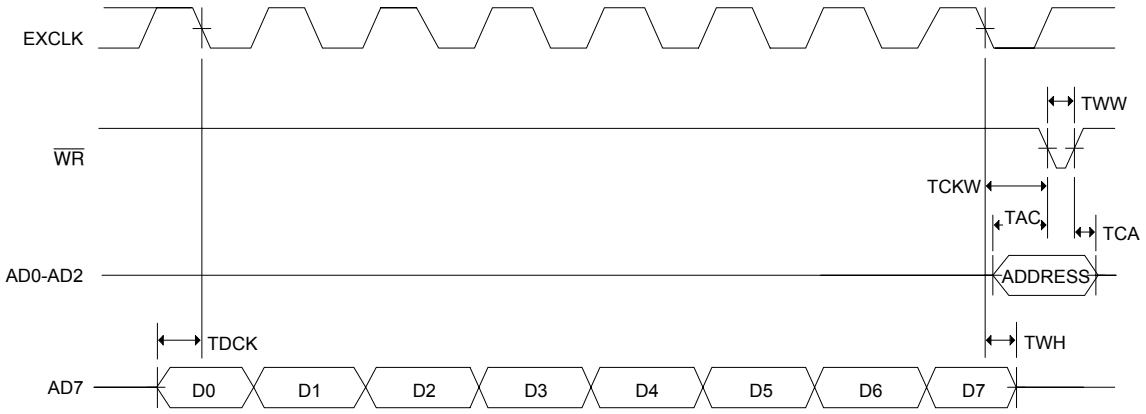
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

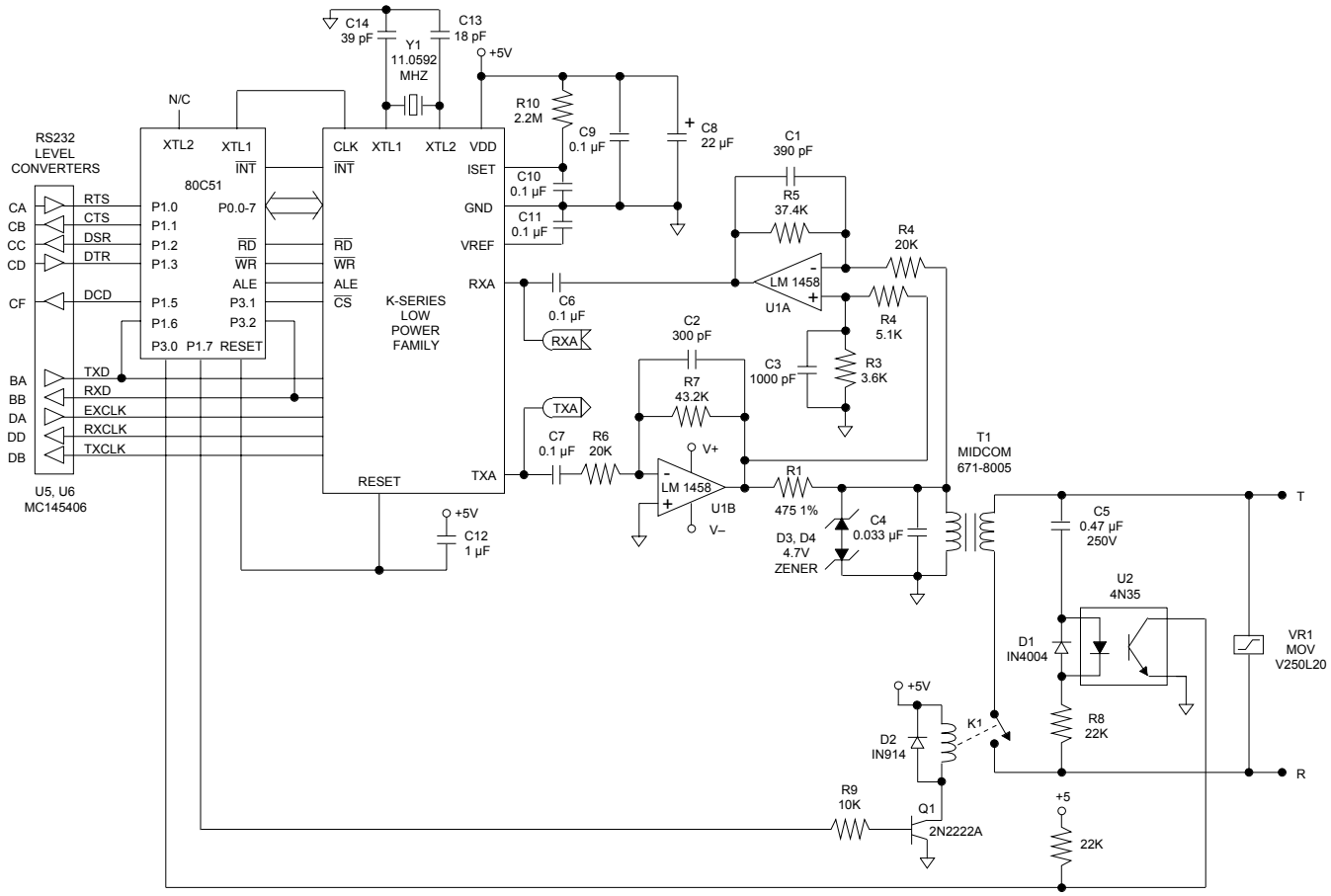


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

TDK Semiconductor's 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

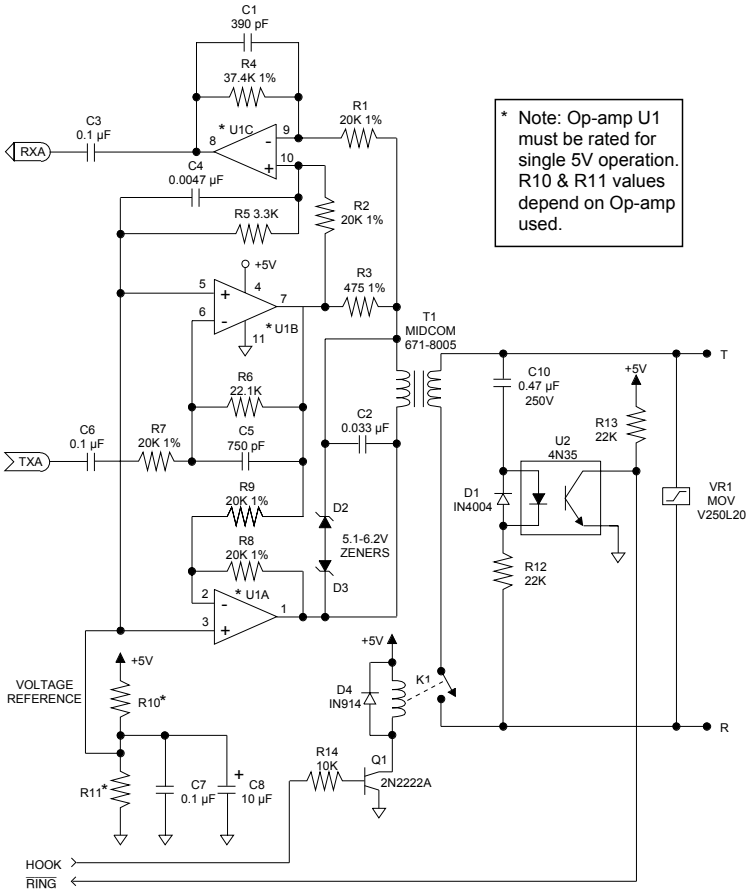


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

USING THE SERIAL MODE ON THE 73K222AL

A sensitivity to specific patterns being written to the control registers in the 73K212/221/222AL and 73K222BL modem data pumps has been seen on some parts when used in the serial control interface mode. An alternating pattern followed by its complement can cause the registers to not have the intended data correctly written to the registers. Specifically, if an alternating ..1010.. pattern is followed by its compliment, ..0101.., the register may instead be programmed with a ..0001.. pattern. After analysis, it has been found that any normal programming sequence should not include these steps with one exception, and that is in DTMF dialing. Since any random DTMF sequence could be dialed, there is the potential for these patterns to appear. For example, if a DTMF digit "5" , 0101 bin is followed by a DTMF digit "0" , 1010 bin, some parts will instead transmit a DTMF digit "8", 1000 bin, in its place. The solution to this problem is to always clear the DTMF bits, D3-D0, between dialed digits. This will not add additional time to dialing since there is ample time between digits when the DTMF bits can be cleared. Previously during the DTMF off time the next digit would be loaded into the TONE register. It is now recommended to first clear bits D3-D0, then the next digit to be dialed is loaded into the DTMF bits.
As mentioned earlier, under normal circumstances these patterns would not be programmed for other registers. If for some reason other registers are programmed in such a way that an alternating pattern is followed by its compliment, those bits should be cleared before the complimentary pattern is sent.
This method has been tested over the entire voltage and temperature operating ranges. It has been found to be a reliable procedure to ensure the correct patterns are always programmed.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit

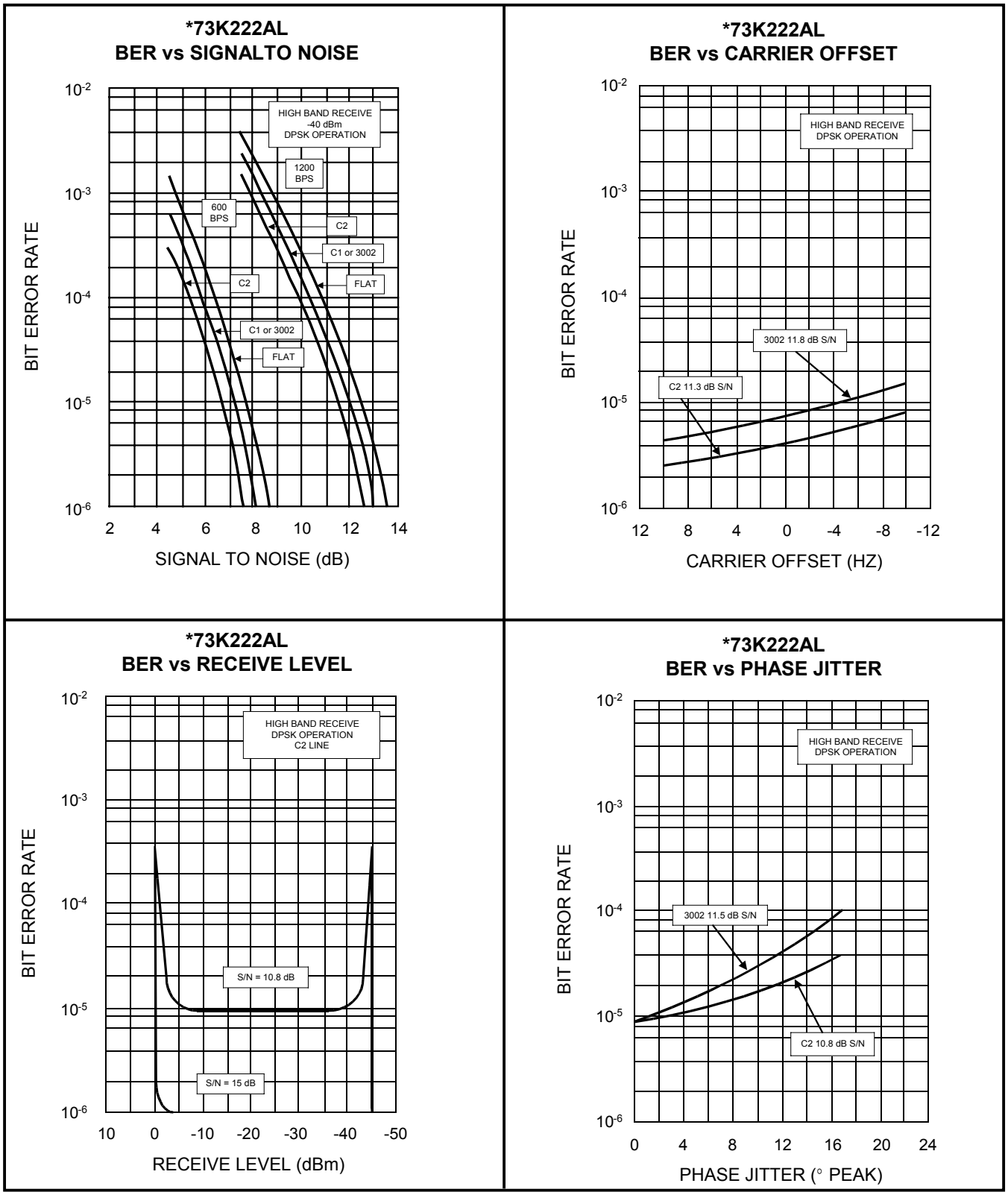
pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

BER vs. Receive Level

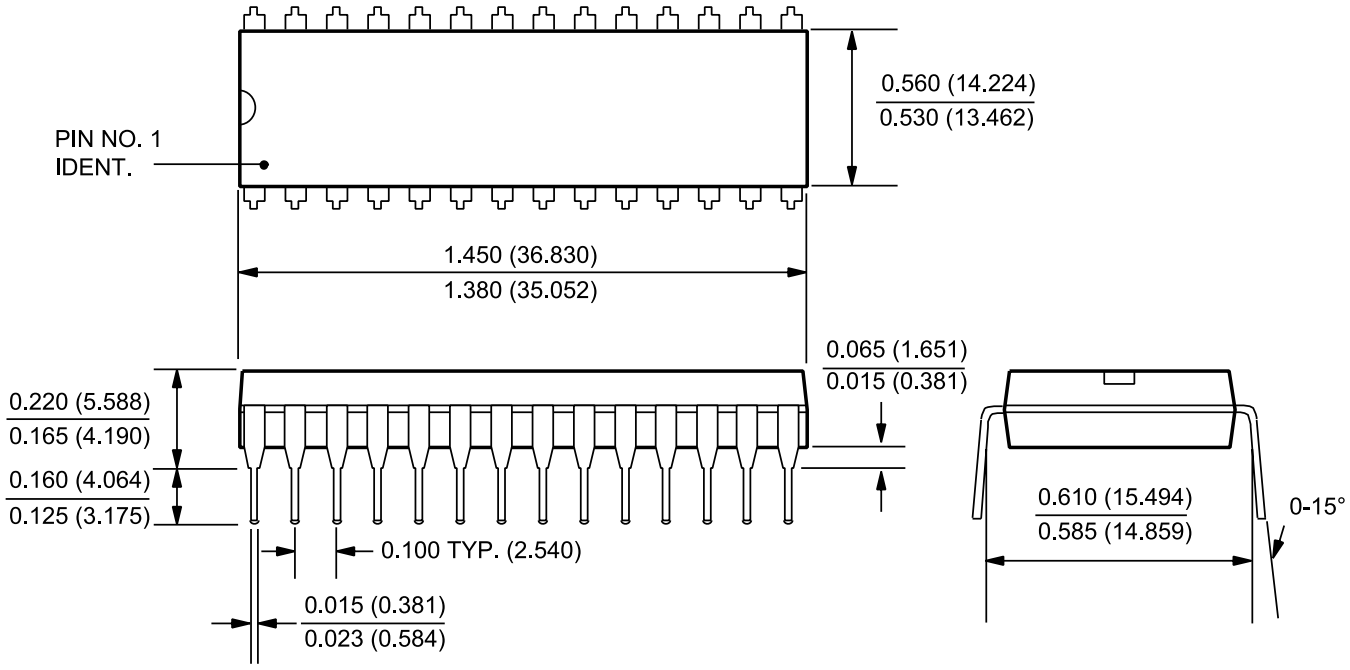
This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the “bowl” of these curves, taken at the BER point, is the measure of dynamic range.



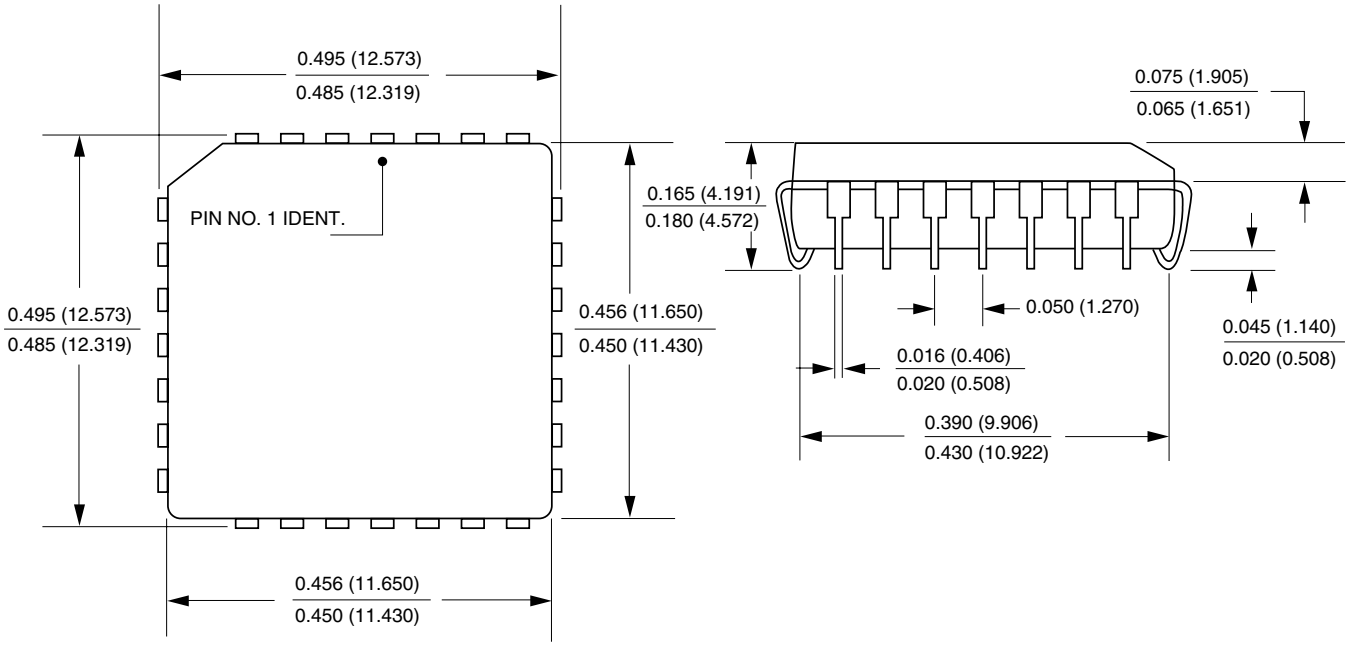
* = “EQ On” Indicates bit CR1 D4 is set for additional phase equalization.

MECHANICAL SPECIFICATIONS

28-Pin DIP



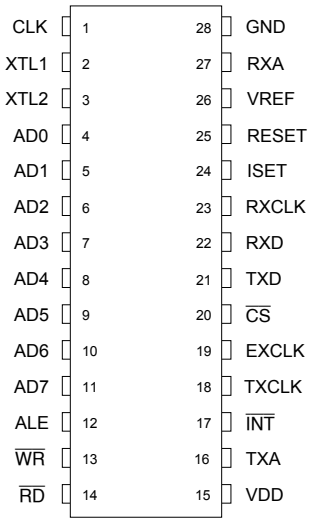
28-Pin PLCC



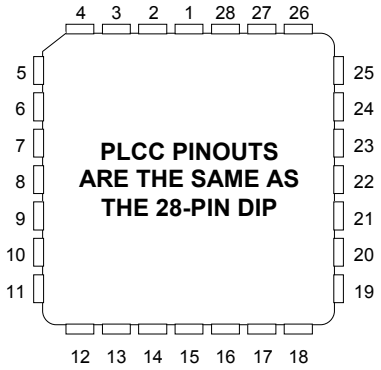
PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



600-Mil
28-Pin DIP
73K222AL-IP



28-Pin PLCC
73K222AL-IH

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
73K222AL with Parallel Bus Interface		
28-Pin Plastic Dual In-Line	73K222AL-IP	73K222AL-IP
28-Pin Plastic Leaded Chip Carrier	73K222AL-IH	73K222AL-IH

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