19-2658; Rev 1; 10/04

Low-Cost, Voltage-Output, 16-Bit DACs in µMAX

General Description

The MAX5204–MAX5207 serial input, voltage-output 16-bit digital-to-analog converters (DACs) provide monotonic 16-bit output over temperature without any adjustments. The MAX5204/MAX5205 operate from a +5V single power supply and use an external reference ranging from +4V to V_{DD}, while the MAX5206/MAX5207 operate from a +3V or +3.3V single power supply and use an external reference ranging from +2V to V_{DD}. The MAX5204–MAX5207 DAC output range is typically from 0 to V_{DD}.

The MAX5204–MAX5207 feature a hardware reset input ($\overline{CLR}$) that when pulled low clears the output to zero code 0000 hex (MAX5205/MAX5207) or resets the output to midscale code 8000 hex (MAX5204/MAX5206).

The 3-wire serial interface is compatible with SPI™/QSPI™/MICROWIRE™. All devices have a low-power shutdown mode that reduces the supply current consumption to 1µA.

The MAX5204–MAX5207 are available in a space-saving 10-pin µMAX® package and are guaranteed over the extended temperature range (-40°C to +105°C). Refer to the MAX5200–MAX5203 data sheet for internal reference versions.

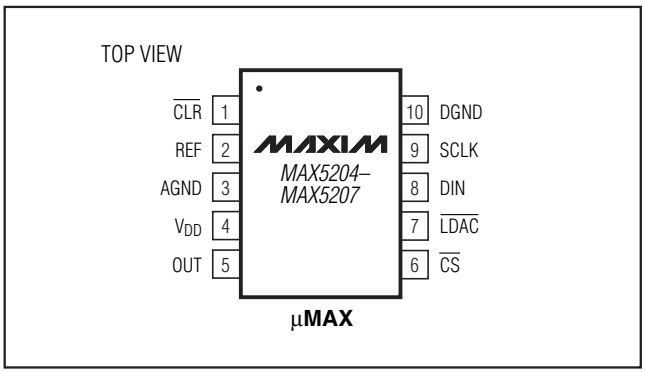
Applications

Low-Cost VCO/VCXO Frequency Control

Industrial Process Control

High-Resolution Offset Adjustment

Pin Configuration



Features

- **Guaranteed 16-Bit Monotonic**
- **10-Pin 5mm × 3mm µMAX Package**
- **Rail-to-Rail Output Amplifier**
- **Single-Supply Operation**
  +5V (MAX5204/MAX5205)
  +3V, +3.3V (MAX5206/MAX5207)
- **Low Power Consumption: 0.5mA**
- **Shutdown Mode Reduces Supply Current to 1µA**
- **SPI/QSPI/MICROWIRE-Compatible 3-Wire Serial Interface**
- **Power-On-Reset Sets Output to**
  Midscale (MAX5204/MAX5206)
  Zero-Scale (MAX5205/MAX5207)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5204AEUB	-40°C to +105°C	10 µMAX
MAX5204BEUB	-40°C to +105°C	10 µMAX
MAX5204ACUB	0°C to +70°C	10 µMAX
MAX5205AEUB	-40°C to +105°C	10 µMAX
MAX5205BEUB	-40°C to +105°C	10 µMAX
MAX5205ACUB	0°C to +70°C	10 µMAX
MAX5206AEUB	-40°C to +105°C	10 µMAX
MAX5206BEUB	-40°C to +105°C	10 µMAX
MAX5206ACUB	0°C to +70°C	10 µMAX
MAX5207AEUB	-40°C to +105°C	10 µMAX
MAX5207BEUB	-40°C to +105°C	10 µMAX
MAX5207ACUB	0°C to +70°C	10 µMAX

Selector Guide appears at end of data sheet.

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MICROWIRE is a trademark of National Semiconductor Corp.

µMAX is a registered trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND .....-0.3V to +6V
AGND to DGND .....-0.3V to +0.3V
REF, OUT to AGND .....-0.3V to (V_{DD} + 0.3V)
$\overline{CLR}$, $\overline{LDAC}$, SCLK, DIN, $\overline{CS}$ to DGND .....-0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444.4mW

Operating Temperature Ranges
MAX520_CUB .....0°C to +70°C
MAX520_EUB .....-40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5204/MAX5205

(V_{DD} = +4.75V to +5.25V, f_{SCLK} = 10MHz (50% duty cycle), V_{REF} = 4.096V, output load = 10kΩ in parallel with 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)						
Resolution	N		16			Bits
Integral Nonlinearity (Note 2)	INL	MAX520_AEUB		±10	±20	LSB
		MAX520_ACUB		±10	±20	
		MAX520_BEUB		±20	±40	
Differential Nonlinearity (Note 2)	DNL	MAX520_A_UB (Note 3)			±1	LSB
		MAX520_BEUB (0°C to +105°C) (Note 3)			±1	
		MAX520_BEUB (-40°C to 0°C)			±2	
Offset Error		Inferred from measurement at 1C00 hex and FFFF hex		±3	±25	mV
Gain Error	GE	Within DAC output range (Note 4)		±0.01	±1	%FSR
Offset Temperature Coefficient				1.5		µV/°C
Gain Temperature Coefficient				3		ppm of FSR/°C
Power-Supply Rejection	PSR	V_{DD} = 5V ±5%, midscale input		±0.06	±0.5	mV/V
DYNAMIC PERFORMANCE						
DAC Output Range		(Note 2)		0 to V_{DD}		V
Output-Voltage Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1LSB of FS, V_{STEP} = 0.25 × V_{REF} to 0.75 × V_{REF}		25		µs
Output Noise		DAC code = 8400 hex, 10kHz		120		nV/√Hz
DAC Glitch Impulse		Major carry transition (code 7FFF hex to code 8000 hex)		10		nV·s
Digital Feedthrough		Code = 0000 hex; $\overline{CS}$ = V_{DD}; $\overline{LDAC}$ = 0; SCLK, DIN = 0 or V_{DD}		10		nV·s
Wake-Up Time		From software shutdown to 90% of output code = FFFF hex		50		µs
Power-Up Time		From power applied to 90% of output code = FFFF hex		10		ms

ELECTRICAL CHARACTERISTICS—MAX5204/MAX5205 (continued)

(V_{DD} = +4.75V to +5.25V, f_{SCLK} = 10MHz (50% duty cycle), V_{REF} = 4.096V, output load = 10kΩ in parallel with 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT						
V_{REF} Input Range			4.0		V_{DD}	V
V_{REF} Input Current				40		µA
V_{REF} Input Resistance				100		kΩ
Input Capacitance				18		pF
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{CLR}$, $\overline{LDAC}$)						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}			200		mV
Input Leakage	I_{IN}	Digital inputs = 0 or V_{DD}			±1	µA
Input Capacitance	C_{IN}			15		pF
POWER REQUIREMENTS						
Positive Power Supply	V_{DD}		4.75		5.25	V
Positive Supply Current	I_{DD}	All digital inputs at 0 or V_{DD} (Note 5)		0.8	1.5	mA
Shutdown Supply Current	I_{SHDN}	All digital inputs at 0 or V_{DD}		1	10	µA
TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}				10	MHz
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Ignore	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Ignore	t_{CS1}		40			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}		40			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Low Setup	t_{LDACS}		40			ns
SCLK Fall to $\overline{CS}$ Fall Ignore	t_{CSOL}		10			ns
$\overline{CS}$ Pulse Width Low for Shutdown	t_{CSWL}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSWH}		100			ns

ELECTRICAL CHARACTERISTICS—MAX5206/MAX5207

(V_{DD} = +2.7V to +3.6V, f_{SCLK} = 10MHz (50% duty cycle), V_{REF} = 2.048V, output load = 10kΩ in parallel with 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)						
Resolution	N		16			Bits
Integral Nonlinearity (Note 2)	INL	MAX520_AEUB		±10	±20	LSB
		MAX520_ACUB		±10	±20	
		MAX520_BEUB		±20	±40	
Differential Nonlinearity (Note 2)	DNL	MAX520_A_UB (Note 3)			±1	LSB
		MAX520_BEUB (0°C to +105°C) (Note 3)			±1	
		MAX520_BEUB (-40°C to 0°C)			±2	
Offset Error		Inferred from measurement at 3800 hex and FFFF hex		±3	±25	mV
Gain Error	GE	Within DAC output range (Note 4)		±0.01	±1.0	%FSR
Offset Temperature Coefficient				1.5		µV/°C
Gain Temperature Coefficient				3		ppm of FSR/°C
Power-Supply Rejection	PSR	V_{DD} = 3V ±10%, midscale input		±0.06	±0.5	mV/V
DYNAMIC PERFORMANCE						
DAC Output Range		(Note 2)		0 to V_{DD}		V
Voltage-Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1LSB of FS, V_{STEP} = 0.25 × V_{REF} to 0.75 × V_{REF}		25		µs
Output Noise		Code = 8400 hex, 10kHz		120		nV/√Hz
DAC Glitch Impulse		Major carry transition (code 7FFF hex to code 8000 hex)		10		nV·s
Digital Feedthrough		Code = 0000 hex; $\overline{CS}$ = V_{DD}; $\overline{LDAC}$ = 0; SCLK, DIN = 0 or V_{DD}		10		nV·s
Wake-Up Time		From software shutdown to 90% of output code = FFFF hex		50		µs
Power-Up Time		From power boosting to 90% of output code = FFFF hex		10		ms
REFERENCE INPUT						
V_{REF} Input Range			2.0		V_{DD}	V
V_{REF} Input Current				20		µA
V_{REF} Input Resistance				100		kΩ
Input Capacitance				18		pF

ELECTRICAL CHARACTERISTICS—MAX5206/MAX5207 (continued)

(V_{DD} = +2.7V to +3.6V, f_{SCLK} = 10MHz (50% duty cycle), V_{REF} = 2.048V, output load = 10kΩ in parallel with 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

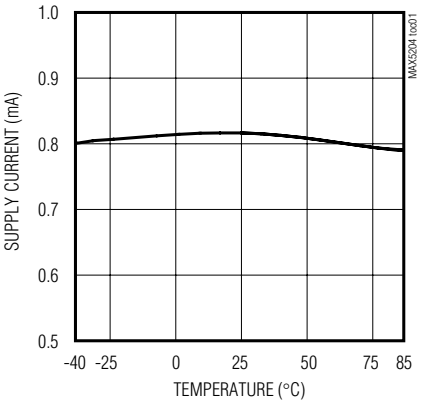
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{CLR}$, $\overline{LDAC}$)						
Input High Voltage	V_{IH}		2.1			V
Input Low Voltage	V_{IL}				0.6	V
Input Hysteresis	V_{HYST}			200		mV
Input Leakage	I_{IN}	Digital inputs = 0 or V_{DD}			±1	µA
Input Capacitance	C_{IN}			15		pF
POWER REQUIREMENTS						
Positive Power Supply	V_{DD}		2.7		3.6	V
Positive Supply Current	I_{DD}	All digital inputs at 0 or V_{DD} (Note 5)		0.5	1.5	mA
Shutdown Supply Current	I_{SHDN}	All digital inputs at 0 or V_{DD}		1	10	µA
TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}				10	MHz
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Ignore	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Ignore	t_{CS1}		40			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}		40			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Low Setup	t_{LDACS}		40			ns
SCLK Fall to $\overline{CS}$ Fall Ignore	t_{CSOL}		10			ns
$\overline{CS}$ Pulse Width Low for Shutdown	t_{CSWL}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSWH}		100			ns

Note 1: Static performance tested at V_{DD} = +5.0V (MAX5204/MAX5205) and at V_{DD} = +3.0V (MAX5206/MAX5207).
Note 2: INL and DNL are guaranteed for outputs between 0.5V to (V_{DD} - 0.5V).
Note 3: Guaranteed monotonic.
Note 4: V_{REF} = 4.096V (MAX5204/MAX5205) and V_{REF} = 2.048V (MAX5206/MAX5207).
Note 5: R_L = ∞, digital inputs are at V_{DD} or DGND.

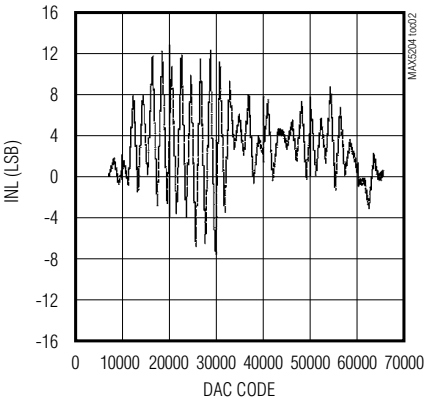
Typical Operating Characteristics

(V_{DD} = +5V, V_{REF} = 4.096V, T_A = +25°C, unless otherwise noted.)

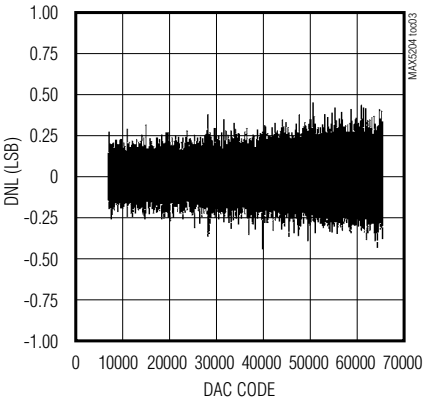
SUPPLY CURRENT vs. TEMPERATURE



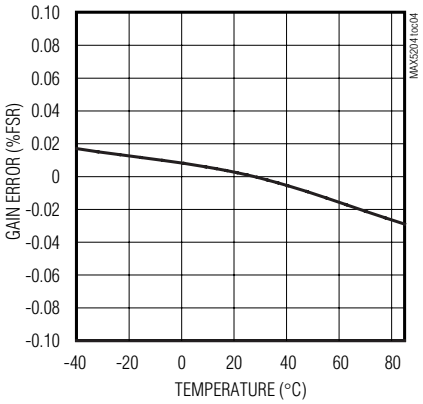
INTEGRAL NONLINEARITY vs. CODE (A GRADE)



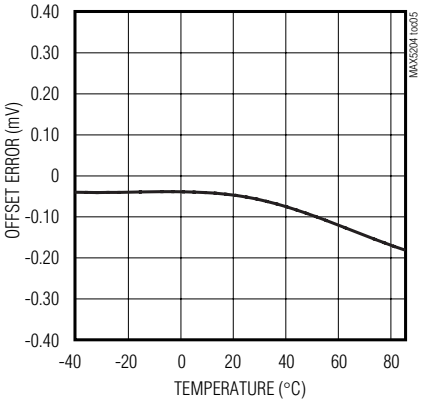
DIFFERENTIAL NONLINEARITY vs. CODE



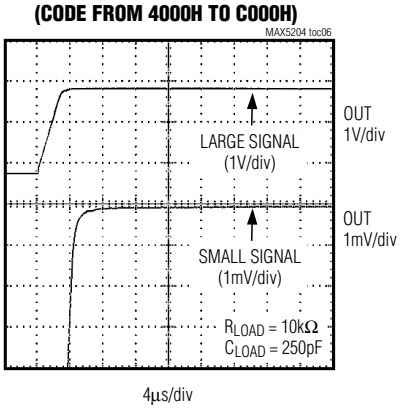
GAIN ERROR vs. TEMPERATURE



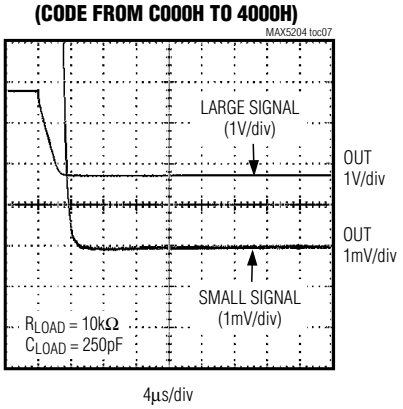
OFFSET ERROR vs. TEMPERATURE



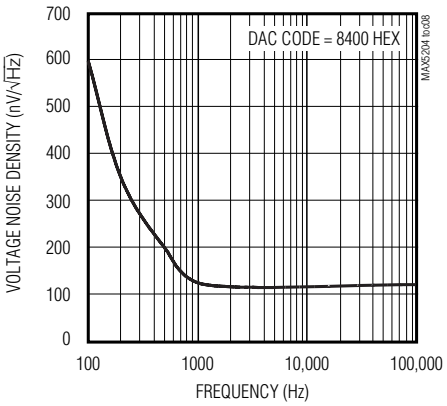
HALF-SCALE OUTPUT SETTLING TIME (CODE FROM 4000H TO C000H)



HALF-SCALE OUTPUT SETTLING TIME (CODE FROM C000H TO 4000H)



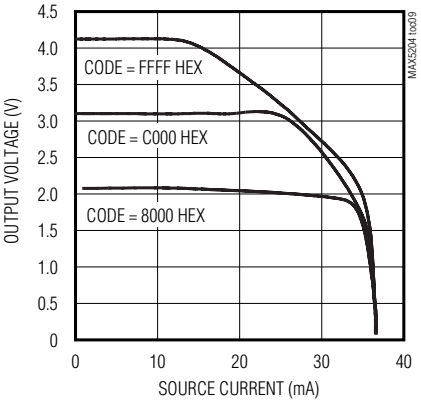
OUTPUT NOISE DENSITY vs. FREQUENCY



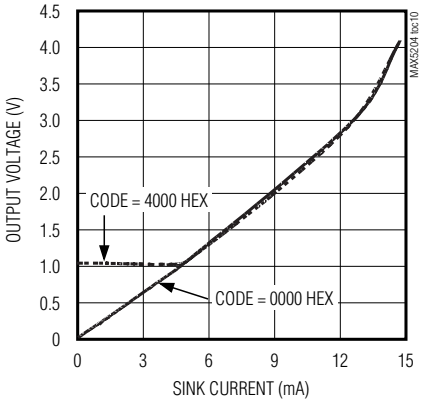
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{REF} = 4.096V, T_A = +25°C, unless otherwise noted.)

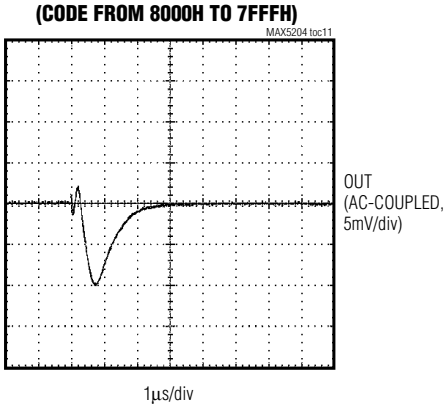
SOURCE-CURRENT CAPABILITY



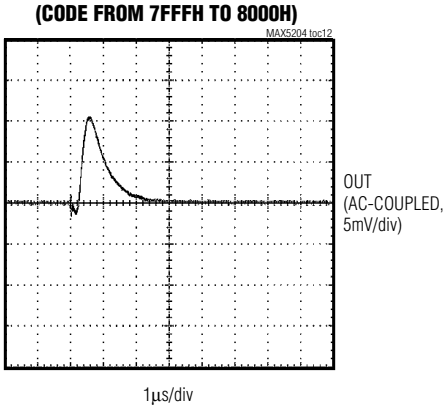
SINK-CURRENT CAPABILITY



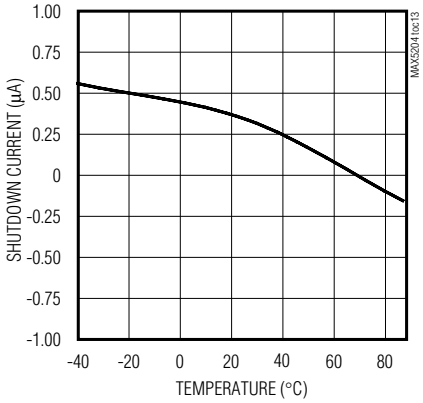
MAJOR-CARRY OUTPUT GLITCH (CODE FROM 8000H TO 7FFFH)



MAJOR-CARRY OUTPUT GLITCH (CODE FROM 7FFFH TO 8000H)



SHUTDOWN CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	$\overline{CLR}$	Reset DAC Active-Low Input. Pull $\overline{CLR}$ low to reset the DAC output to midscale output (8000 hex) for MAX5204/MAX5206 and to zero-scale output (0000 hex) for MAX5205/MAX5207. For normal operation, connect $\overline{CLR}$ to V_{DD}.
2	REF	External Reference Voltage Input
3	AGND	Analog Ground
4	V_{DD}	Positive Supply Voltage. Bypass V_{DD} to AGND with a 10µF capacitor in parallel with a 0.1µF capacitor.
5	OUT	DAC Output Voltage
6	$\overline{CS}$	Active-Low Chip-Select Input
7	$\overline{LDAC}$	Load DAC Input
8	DIN	Serial Data Input
9	SCLK	Serial Clock Input. Duty cycle must be 40% to 60%.
10	DGND	Digital Ground

Detailed Description

The MAX5204–MAX5207 serial 16-bit, voltage-output DACs are easily configured with a 3-wire serial interface. These devices offer full 16-bit performance with less than ±20LSB integral linearity error and less than ±1LSB differential linearity error, thus ensuring monotonic performance. Serial data transfer minimizes the number of package pins required. The MAX5204–MAX5207 include control-logic circuitry, a 16-bit data-in shift register, and a DAC register. The MAX5204–MAX5207 output is buffered and the full-scale output voltage is V_{REF} (typ).

The MAX5204–MAX5207 feature a hardware reset input ($\overline{CLR}$) that when pulled low clears the DAC output to zero code 0000 hex (MAX5205/MAX5207) or resets the DAC output to midscale code 8000 hex (MAX5204/MAX5206). For normal operation, connect $\overline{CLR}$ to V_{DD}.

Reference Input

The MAX5204/MAX5205 (+5V supply) use an external reference between 4V to V_{DD}, while the MAX5206/MAX5207 (+3V supply) use an external reference from 2V to V_{DD}. The DAC output range is from 0 to V_{REF}.

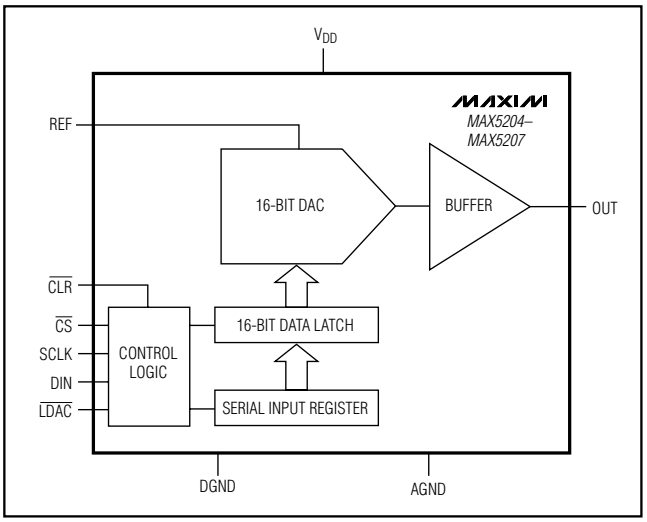


Figure 1. MAX5204–MAX5207 Simplified Functional Diagram

Digital Interface

The MAX5204–MAX5207 digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE and most DSP interfaces. All of the digital input pins ($\overline{CS}$, SCLK, DIN, $\overline{CLR}$, and $\overline{LDAC}$) are TTL compatible. SCLK can accept clock frequencies as high as 10MHz for a +5V supply and 10MHz for a +3V or +3.3V supply.

One of two methods can be used when interfacing and updating the MAX5204–MAX5207. The first requires

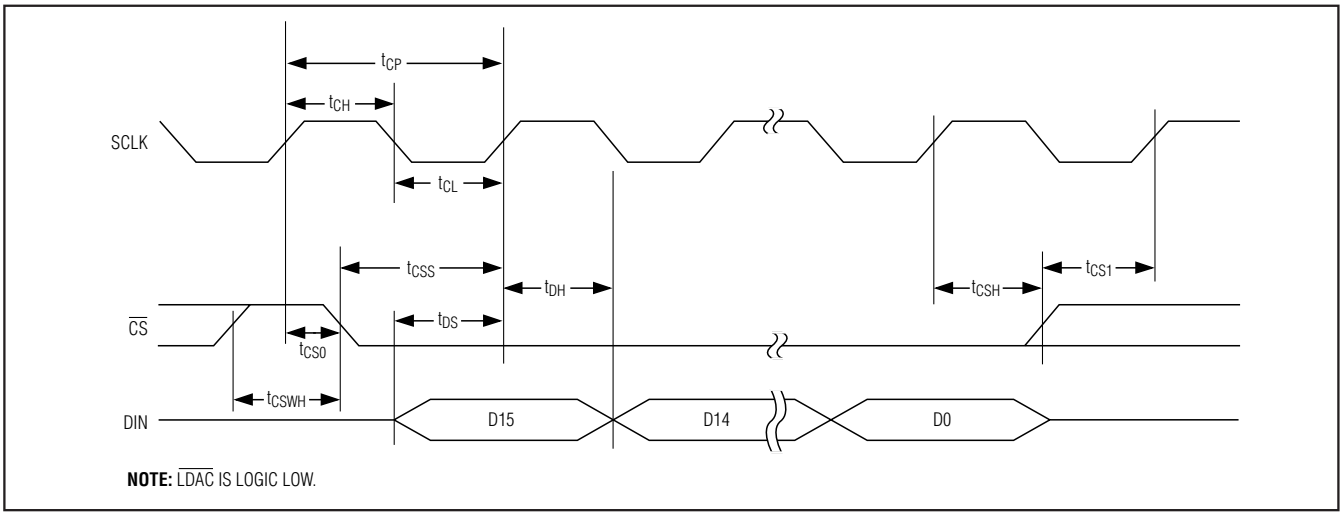


Figure 2. 3-Wire Interface Timing Diagram

three digital inputs: $\overline{CS}$, DIN, and SCLK (Figure 2). The active-low chip-select input ($\overline{CS}$) enables the serial data loading at the data input (DIN). Pull $\overline{CS}$ low and clock in each bit of the 16-bit digital word on the rising edge of the serial clock (SCLK). Two eight-bit bytes can be used, and do not require any additional time between them. Pulling $\overline{CS}$ high after loading the 16-bit word transfers that code into the DAC register and then updates the output. If $\overline{CS}$ is not kept low during the entire loading of the 16-bit word, data will be corrupted. In this case, a new 16-bit word must be loaded. $\overline{LDAC}$ must be kept low at all times for the above instructions.

An alternate method of interfacing and updating the MAX5204–MAX5207 can be done with a fourth digital input, the active-low load DAC ($\overline{LDAC}$). $\overline{LDAC}$ allows the output to update asynchronously after $\overline{CS}$ goes high. It is useful when updating multiple MAX5204–MAX5207s synchronously when sharing a single $\overline{LDAC}$ and $\overline{CS}$ line. $\overline{LDAC}$ must be kept high at all times during the data loading sequence and must only be asserted when $\overline{CS}$ is high. Asserting $\overline{LDAC}$ when $\overline{CS}$ is low can cause corrupted data. To operate the MAX5204–MAX5207 using $\overline{LDAC}$, pull $\overline{LDAC}$ high, pull $\overline{CS}$ low, load the 16-bit word as described in the previous paragraph, and pull $\overline{CS}$ high again. Following these commands, the DAC output only updates when $\overline{LDAC}$ is asserted low (Figure 3).

Shutdown Mode

The low-power shutdown mode reduces supply current to typically 1µA and a maximum of 10µA. Shutdown mode is not activated through command words, as is common among D/A converters. These devices require careful manipulation of $\overline{CS}$ and SCLK (Figure 4).

Shutting Down

To shut down the MAX5204–MAX5207, change the state of SCLK (either a high to low or low to high transition can be used) and pulse two falling $\overline{CS}$ edges. In order to keep the device in shutdown mode, SCLK **must** not change state. SCLK must remain in the state it is in after the two $\overline{CS}$ pulses.

Waking Up

There are two methods to wake up the MAX5204–MAX5207. Pulse one falling $\overline{CS}$ edge or transition SCLK. It takes 50µs typically from the $\overline{CS}$ falling edge or SCLK transition for the DAC to return to normal operation.

Power-On Reset

The MAX5204–MAX5207 have a power-on reset circuit to set the DAC's output to a known state when V_{DD} is first applied. The MAX5204/MAX5206 reset to midscale (code 8000 hex) upon power-up. The MAX5205/MAX5207 reset to zero-scale (code 0000 hex) upon power-up. This ensures that unwanted output voltages do not occur immediately following a system power-up, such as a loss of power. It is required to apply V_{DD} first before any other input (DIN, SCLK, $\overline{CLR}$, $\overline{LDAC}$, $\overline{CS}$, and REF).

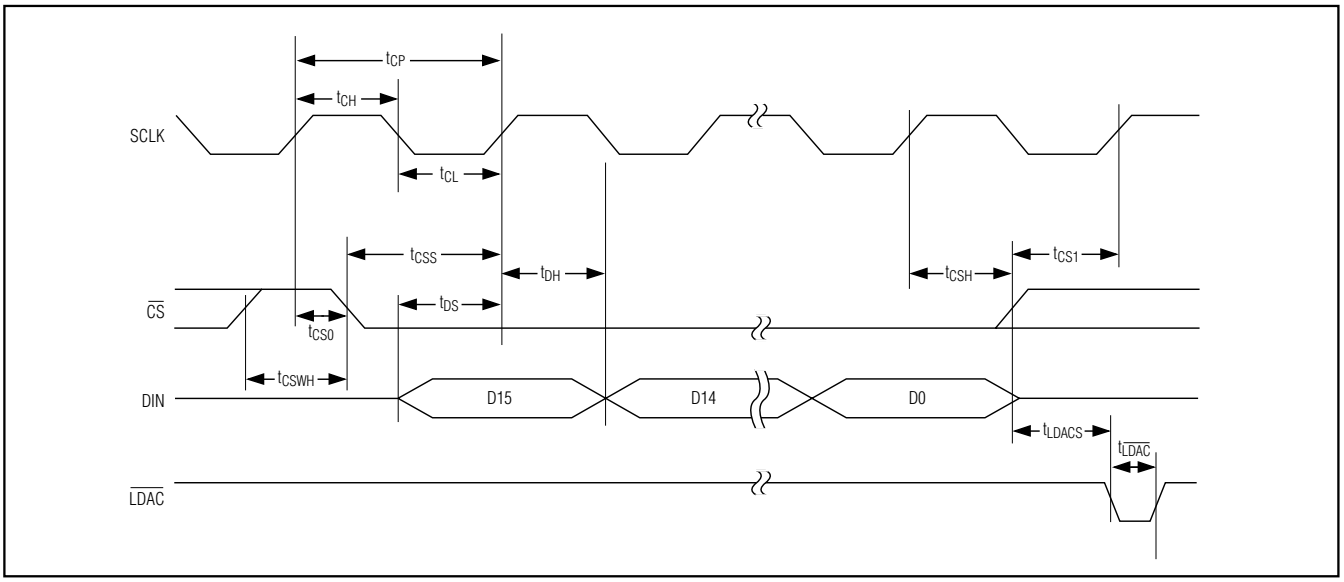


Figure 3. 4-Wire Interface Timing Diagram

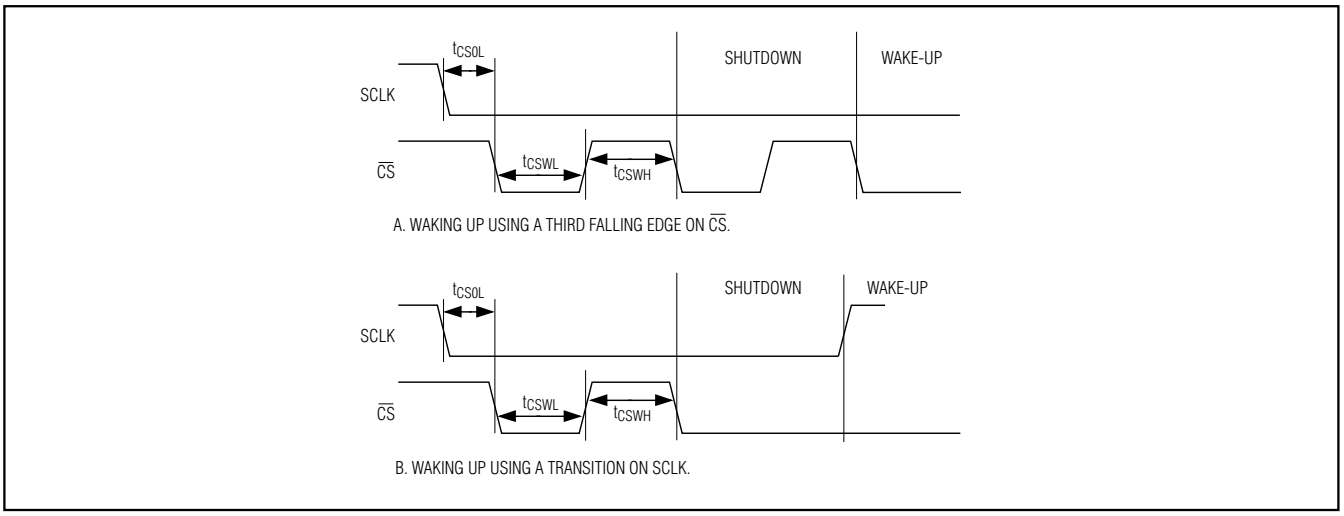


Figure 4. Shutdown Timing

Applications Information

Power Supply and Bypassing Considerations

Bypass the power supply with a 10µF capacitor in parallel with a 0.1µF capacitor to AGND. Minimize lead lengths to reduce lead inductance. If noise becomes an issue, use shielding and/or ferrite beads to increase isolation.

Output Buffer

The MAX5204–MAX5207 include low-offset, low-noise buffers enabling the output to source 15mA or sink 5mA. The output buffer operates at a slew rate of 0.6V/µs. With a 1/4 FS to 3/4 FS output transition, the buffer output typically settles to 1LSB in about 25µs. The MAX5204–MAX5207 output buffers provide a low 0.2Ω typical output impedance. The MAX5204–MAX5207 buffer amplifiers typically produce 120nV/√Hz noise at 10kHz.

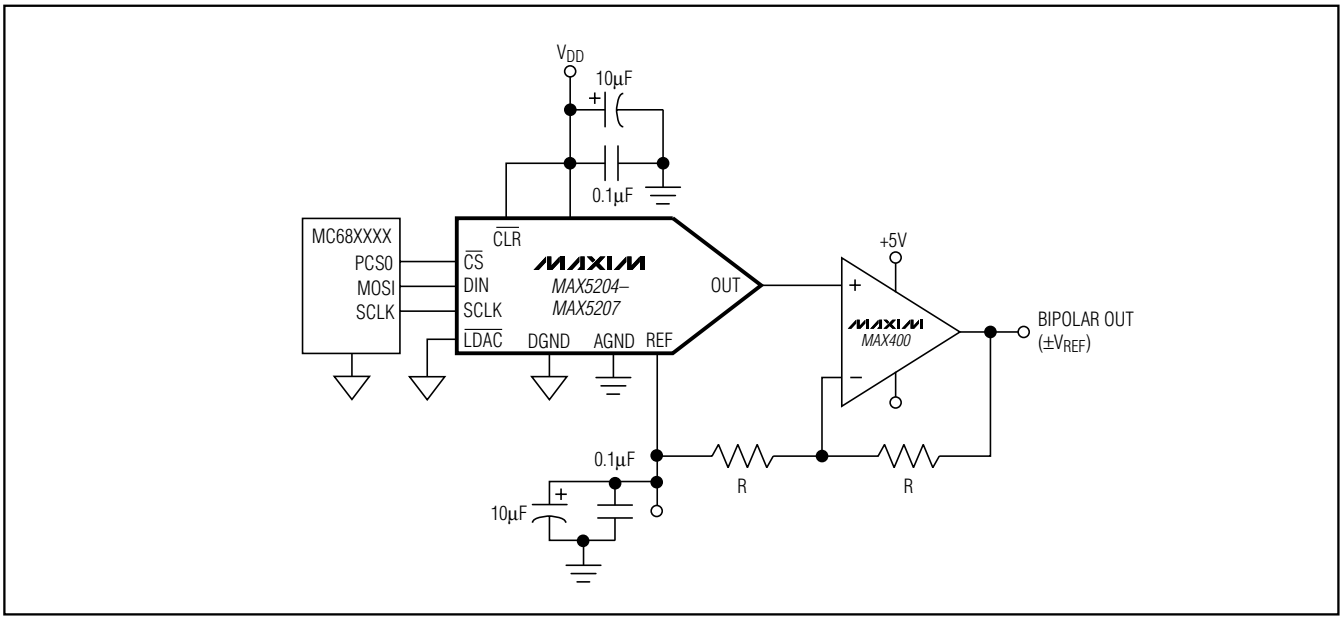


Figure 5. MAX5204–MAX5207 Typical Operating Circuit—Bipolar Output

Table 1. Bipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	$+V_{REF} \times (32{,}767 / 32{,}768)$
1000 0000 0000 0001	$+V_{REF} \times (1 / 32{,}768)$
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF} \times (1 / 32{,}768)$
0000 0000 0000 0000	$-V_{REF} \times (32{,}768 / 32{,}768)$

Bipolar Configuration

The MAX5204–MAX5207 are designed for unipolar operation, but can be used in bipolar applications with an external amplifier and resistors. Figure 5 shows the MAX5204–MAX5207 configured for bipolar operation. The op amp is set for unity gain. Table 1 lists the offset binary code for this circuit. Output voltage range is $\pm V_{REF}$.

Layout Considerations

Digital and AC transient signals coupling to AGND can create noise at the output. Connect AGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane. Wire-wrapped boards and sockets are not recommended. For optimum system performance, use printed circuit (PC) boards with separate analog and digital ground planes. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND pins together at the IC. The best ground connection is achieved by connecting the DAC's DGND and AGND together, and then connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise can get through the DAC's analog portion.

Chip Information

TRANSISTOR COUNT: 8764

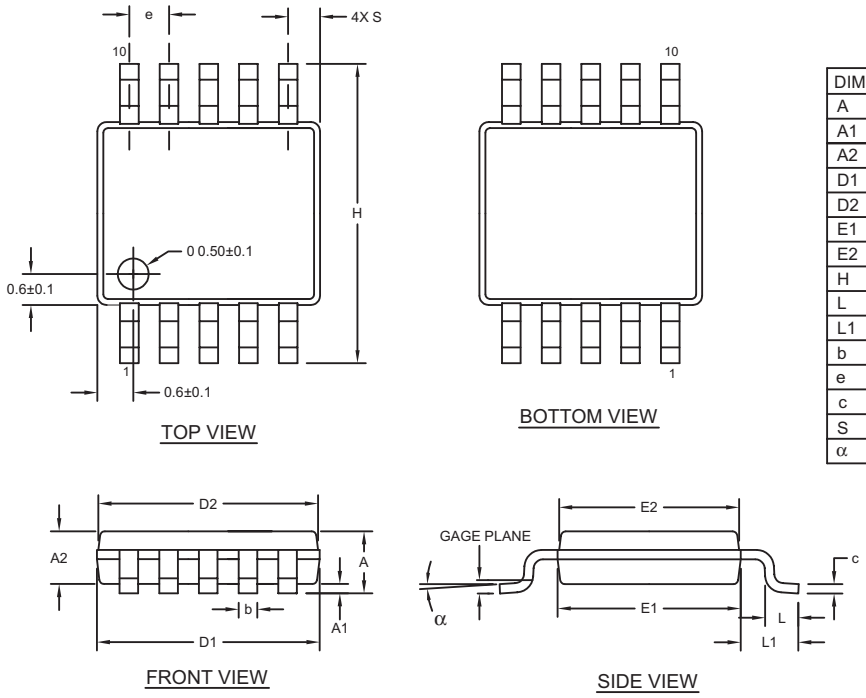
PROCESS: BiCMOS

Selector Guide

PART	INTEGRAL NONLINEARITY (LSB MAX)	SUPPLY VOLTAGE RANGE (V)	REFERENCE INPUT RANGE (V)	POWER-ON-RESET VALUE
MAX5204AEUB	20	4.75 to 5.25	4 to V_{DD}	Midscale
MAX5204ACUB	20	4.75 to 5.25	4 to V_{DD}	Midscale
MAX5204BEUB	40	4.75 to 5.25	4 to V_{DD}	Midscale
MAX5205AEUB	20	4.75 to 5.25	4 to V_{DD}	Zero
MAX5205ACUB	20	4.75 to 5.25	4 to V_{DD}	Zero
MAX5205BEUB	40	4.75 to 5.25	4 to V_{DD}	Zero
MAX5206AEUB	20	2.7 to 3.6	2 to V_{DD}	Midscale
MAX5206ACUB	20	2.7 to 3.6	2 to V_{DD}	Midscale
MAX5206BEUB	40	2.7 to 3.6	2 to V_{DD}	Midscale
MAX5207AEUB	20	2.7 to 3.6	2 to V_{DD}	Zero
MAX5207ACUB	20	2.7 to 3.6	2 to V_{DD}	Zero
MAX5207BEUB	40	2.7 to 3.6	2 to V_{DD}	Zero

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

10LUMAX.EPS

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

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